Bridge For On-Board and On-Chip 1149.4-Compliant Testability

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Abstract

This paper describes a novel non-invasive technique that exploits the 1149.1 and 1149.4 test access standards for contactless in-circuit continuous monitoring and testing of analog and digital nodes in densely populated, mixed-signal circuit boards with limited nodal access. It also describes a mixed-signal IC core Design-For-Testability infrastructure for testing logic core and embedded memories via boundary-scan circuitry without using the physical probing methods and testers, and with the minimum pin-count access. This paper also introduces a method of in-circuit passive component behavior estimation instead of utilizing more expensive methods for component analog measurement and value calculation.

1. Introduction

As the complexity of today's mixed-signal printed circuit boards (PCB) populated with integrated circuits (IC) and passive elements increases continuously, PCBs get to be more dense and ICs are more complicated and occupied with functions. As a result, it becomes more difficult to perform quick and exhaustive diagnose faults and to debug the circuits after the components was assembled on the PCB.

The increasing trend to integrate greater capability into mixed-signal ICs results in embedded complexities that has significantly reduced the effectiveness of the present in-circuit testing (ICT) or flying probe methods at the PCB level via a direct physical contact interface. The lack of signal probing pads (or test points) on a PCB occurs because ICs are densely assembled on the both sides of state-of-the-art multilayer board. Physical access for manufacturing defects testing is quickly disappearing when Ball-Grid-Array (BGA), Flip Chip or other advanced and leadless package types are assembled. The addition of test pads for probe access greatly increases the board real estate and other PCB mechanical problems. To access analog test points, however, an external and very expensive ICT testers and other test equipment must still be utilized, and the PCB layout and shielding must accommodate external probing. The densely populated, multilayer mixed-signal PCB probing is an ongoing challenge and a high priority need in a board and system functional testing and debug.

Similar situation happens in complex mixed-signal ICs with usage of high-density advanced packaging technologies, such as system-on-chip (SOC), system-in-package (SIP), chip-scale-packaging (CSP) due to physical access limitation to in-core test with accompanying pin count penalty. It is outlined in various papers [1,2], that the combination of 1149.4 standard architecture with the voltage-current measurement methods may compensate the bottlenecks encountered due to the limited access to a PCB nodes or to the core of a complex IC.

The 1149.4 standard has been slow to gain adoption in new ICs, and this issue stimulates some new alternative approaches to analog testability [3]. A probable reason for such situation [4] may be a relative complexity of 1149.4 infrastructure and the impact it would have had on the IC design. After more than one decade of success of pervasive and versatile 1149.1 technology it clearly shows that these favorable circumstances depend upon its acceptability in some supplementary areas, such as the board Design-For-Testability (DFT) rules, on-board programming and in-system configuration tools [5], IC design validation, etc.

This paper will describe a new technique based on the 1149.1 and 1149.4 test access standards for contactless in-circuit AC/DC testing and continuous monitoring of both analog and digital signals in densely populated, mixed-signal PCB with limited nodal access. We further describe a mixed-signal IC on-chip core DFT infrastructure for testing functional core and embedded memories via boundary-scan circuitry without using the physical probing methods and testers and with minimum pin-count access. Before we answer the question of what that means, this paper starts by introducing some basics of the 1149.4 test access infrastructure. Next, a board level usage of the new technique is described and its possible impact of on-board analog testability is discussed. The paper further introduces the new IC core level DFT infrastructure together with the hardware verification description of this new technique based on the usage of the general purpose IC [6] of National Semiconductors. After considering the new method of in-circuit estimation of analog passive elements, it is explained what way this method and the described novel boundary-scan circuitry can be used instead of traditional analog measurement.

2. The 1149.4 infrastructure

Efforts on 1149.1 JTAG standard extension for analog and mixed-signal realm at both IC and PCB in order to implement the contactless signal level or waveform probing, insertion, and in-circuit analog measurements, has resulted in the adoption of the 1149.4 standard in 1999 [7]. The general architecture of an IC designed according to 1149.4 is shown in Fig. 1. The standard requires one or more shift register (Boundary-Scan Register or BSR) cells per IC pin, and shifts boundary-scan data into a BSR via TDI pin and out through TDO pin. The BSR cells may be implemented as a digital boundary modules (D), associated with digital input/output (I/O) pins, or as an Analog Boundary Modules (ABM), associated with analog I/O pins, one ABM per one analog I/O pin. The Test Bus Interface Circuit (TBIC) connects two external analog buses (AT1 and AT2 pins) to two internal test buses (AB1 and AB2). The Test Access Port (TAP) circuitry facilitates both digital and analog boundary scan testing.

The 1149.4 is built as an extension of well-known 1149.1 standard. Both are very similar, but the PROBE instruction is specific and dedicated 1149.4 instruction. The primary purpose of the PROBE execution is to allow continuous-time access to an IC analog pin signals without affecting the mission (or normal functional) mode of the IC. The only restriction is that not more than two analog pins can be sampled at one time through AT1 and AT2 pins. When the PROBE is active, all digital D modules are set to allow digital I/Os to be connected to the IC core circuitry only, so that D modules are not intended for continuous-time access to digital I/Os. All ABMs are set to allow analog I/Os to be connected to the IC core circuitry too, but ABM switch patterns of one or two ABMs are used by the PROBE to connect their I/Os to either or both of the internal AB1/2 buses. The TBIC circuitry switches are also governed to allow AB1/2 to AT1/2 connections and finally I/Os to AT1/2 connections may be made as required through the PROBE execution.

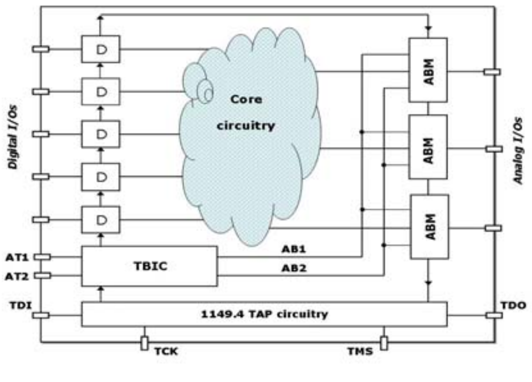

Fig. 1

The example of the PROBE enabling TBIC and ABM switches for Pin 1-to-AT1 signal probing path creation and AT2-to-Pin 2 signal injection path creation is shown in Fig. 2. The content of the TBIC circuitry control register impacts to connect AT1 pin to AB1 bus via switch S5 and to connect AT2 pin to AB2 bus via switch S6. Further, ABM1 switch pattern connects analog probing Pin 1 via switch SB1 to AB1 bus, and ABM2 switch pattern connects analog signal injecting Pin 2 via switch SB2 to AB2 bus. The signal voltage appearing on the PCB in-circuit analog probing Pin 1 (node) can be monitored in real time at the external AT1 pin as a voltage level or waveform. Similarly, the analog test injecting signal that is applied to the external AT2 pin can be conveyed in real time to the PCB in-circuit analog Pin 2 (node) as a signal voltage level or waveform. The IC is staying in its mission mode of operation.

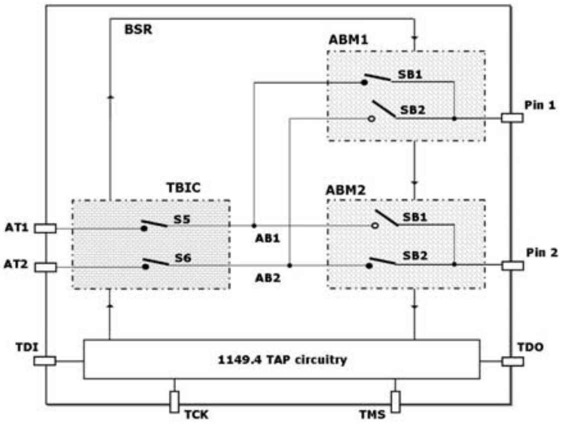

Fig. 2

The 1149.4 architecture today is well described in literature [8,9]. The value and capabilities of the 1149.4 analog test bus itself are proportional to the percentage of ICs on a PCB that are designed to be compliant with the standard [1]. However, the realities of the marketplace could prevent any new standard from being adopted at the IC level until it makes the IC cheaper to manufacture and test, and adding features of the 1149.4 is not addresses analog testing only [10].

3. Bridge for in-circuit board testability

The infrastructure of the novel technique for a mixed-signal PCB testability enhancement, that we call Bridge-For-Testability (BFT), at least that is what the acronym stands for, is depicted in Fig. 3. An objective of this technique is to add and facilitate a “virtual” (contactless) contact for in-circuit node 1149.4-compliant probing, both analog and digital, in a mixed-signal PCB.

As seen in Fig. 3, the BFT IC is provided with a 1149.4-compliant TAP-1 circuitry (Prober) and one additional series 1149.1- or 1149.4-compliant TAP-2 circuitry (Coder). The BSR-1 of the Prober does not include digital boundary modules D, but only TBIC and two analog boundary modules, ABM1 and ABM2, connected respectively to outputs of analog multiplexers Mux1 and Mux2. The BSR-2 of the Coder includes digital boundary modules D or 1149.1-cells connected to address inputs of multiplexers Mux1/2. There is no functional core of the BFT IC but two series boundary-scan circuitries only. It means that the IC does not have any functional usage and is to be assembled on a PCB with the only goal of the testability improvement. The external I/Os of the IC (A_1, A_2, ...) are connected to a PCB in-circuit nodes with restricted physical access, both analog and digital.

The node multiplexers Mux1/2 are provided for selectively connecting either or both of PCB nodes to one or two analog boundary modules (ABM1 and ABM2). The selection accomplished by providing a node selection code in boundary-scan 1149.1 or 1149.4-compliant protocol through BSR-2 of the Coder circuitry. As a function of the node selection address code, the Mux1/2 circuitry connects the selected external IC I/O pin, which is connected to a PCB in-circuit node, via outputs of analog multiplexers Mux1/2, to ABM1/2. Therefore, the 1149.4 standard PROBE instruction via BSR-1 of the Prober circuitry provides connection of the selected I/O pin (PCB in-circuit node) to either or both of the IC (or a PCB) external test buses AT1/2.

When the PCB is in mission mode and the BFT IC is in the “shadow mode” (with no usage), the TAP-1 circuitry of Prober is in a reset state, so that ABM1/2 switches SB1 and SB2 disconnect outputs of analog multiplexers from internal test buses AB1/2, and TBIC switches S5 and S6 disconnect buses AB1/2 from external test buses AT1/2 respectively (Fig. 2). Moreover, the TAP-2 circuitry of Coder is in a reset state too, so outputs of the BSR-2 digital boundary-scan cells, connected to address code inputs of multiplexers, are tri-stated and all external I/Os of the IC (A_1, A_2, ...) are disconnected from multiplexers outputs. There is no impact of BFT IC on the PCB mission mode in this case.

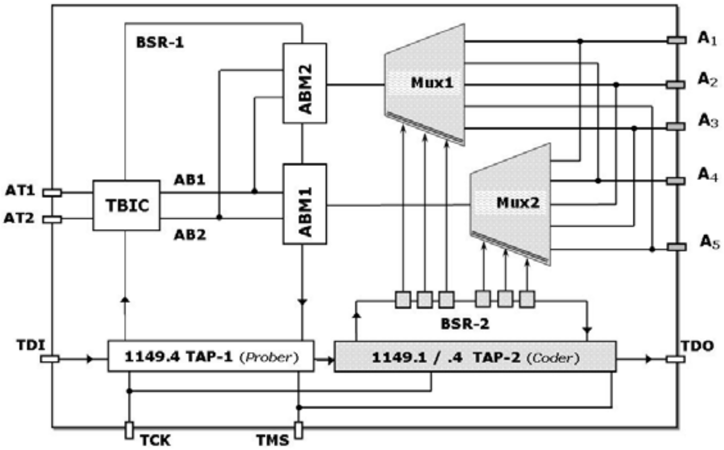

Fig. 3 Bridge-For-Testability structure

When the PCB is in mission mode or test mode and the BFT IC is in the “working mode” initiated by a boundary-scan protocol, the 1149.1- or 1149.4-style sequence to be applied to the external IC TDI pin includes shifting the PRELOAD instruction into the instruction register (IR) of TAP-2 circuitry, followed by address input code of analog multiplexers Mux1/2. These preloaded address code is to be shifted into the BSR-2 and then captured and clamped here as a result of shifting the CLAMP instruction into the IR of TAP-2 circuitry in the same 1149.1 or 1149.4-style sequence. The code applies to the address inputs of analog multiplexers Mux1/2 and defines the external I/Os of the IC (A_1, A_2, ...) that are selected to be multiplexed to one or both of ABM1/2. The PRELOAD - CLAMP instruction sequence does not interrupt mission mode of any boundary-scan device in the scan chain of BFT IC, so does not interrupt the PCB mission mode too. The EXTEST instruction may also be used in this sequence instead of the CLAMP when the PCB is in the test mode.

Then the PROBE instruction is to be shifted into the IR of TAP-1 circuitry of Prober via the same boundary-scan chain of two series TAPs. This instruction enables TBIC switches S5 and S6, as well as one or both of ABM1/2 switches SB1 and SB2 (Fig. 2) for the following signal delivery paths creation, according to analog multiplexer address code preloaded above:

AT1 <-> AB1 <-> ABM1 <-> Mux1 <-> selected external IC I/O pin (A_1, A_2, ...)
AT2 <-> AB2 <-> ABM2 <-> Mux2 <-> selected external IC I/O pin (A_1, A_2, ...)

When the PROBE instruction is executed, either or both of selected external IC I/O pins, both analog and digital, are connected respectively to one or both of external IC pins AT1 and AT2 for sampling or inserting signal levels or waveforms in real time, as well as for analog measurement purposes (see part 6).

4. Bridge for in-core IC testability

The same principle as it was described in the previous part, is used to perform a novel on-chip core DFT infrastructure as depicted in Fig. 4. The core circuitry of a functional IC is wrapped in a test shell of 1149.4-compliant BSR-1 (TAP-1 Prober), that is connected in series to additional 1149.1- or 1149.4-

compliant TAP-2 Coder circuitry with BSR-2. The IC internal boundary-scan chain contains, hence, two serial TAPs.

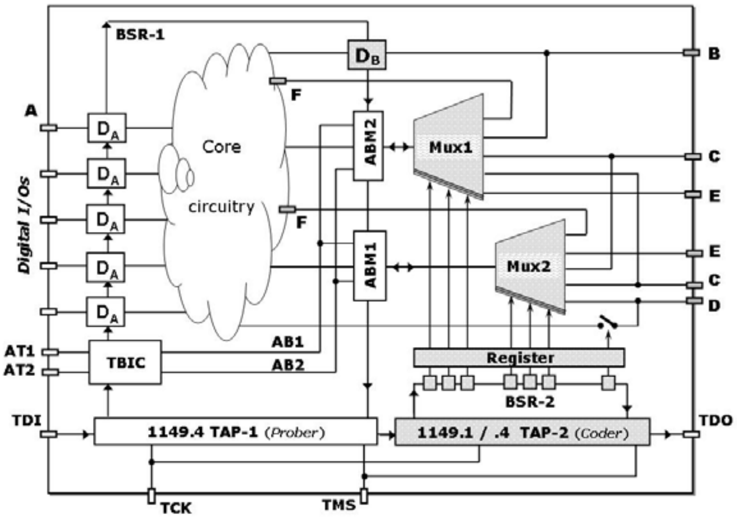

Fig. 4 On-chip mixed-signal core DFT

The BSR-1 of the Prober may include, in addition to TBIC, the following boundary-scan cells:

a) 1149.1- or 1149.4-compliant digital cells (modules) $\mathbf{D_A}$, connected to the regular digital I/O pins (**A**-type pin) of the functional IC ("regular" means 1149.1 or 1149.4 exactly compliant);
b) 1149.4-compliant digital boundary modules $\mathbf{D_B}$, connected to the "1149.4-probeable" digital I/O pins of the functional IC; and
c) analog boundary modules ABM1 and ABM2, connected respectively to analog multiplexers Mux1/2, the number of which is equal to the number of ABMs in BSR-1.

Let's discuss all possible types of I/O pins (in addition to regular **A**-type) the functional IC also includes (Fig. 4).

The **B-type** digital functional I/O pins are connected to analog multiplexers Mux1/2 and to dedicated digital modules $\mathbf{D_B}$. When the IC is in mission mode, **B**-type pins are connected to the IC core via their modules $\mathbf{D_B}$ and disconnected from ABM1/2 according to the proper neutral address provided on multiplexers Mux1/2 address inputs. For in-circuit PCB level test purposes, the **B**-type pins are isolated from the IC core by modules $\mathbf{D_B}$, while being connected to multiplexers, so become to be the "1149.4-probeable" pins that are usable for in-circuit PCB level test purposes, because they are connected to ABM1/2 (according to the proper multiplexer **B**-type pin address) for 1149.4 protocol implementation.

The **C-type** analog functional I/O pins have full 1149.4 support through one or both of ABM1/2 via one or both of multiplexers Mux1/2. These pins are usable both for the in-circuit PCB level test purposes (with PROBE instruction, according to the proper multiplexer **C**-type pin address) and for connection to the IC core via ABM1/2 when the IC is in mission mode.

The **D-type** mixed-signal functional I/O pins (not 1149.4-compliant) are connected to analog multiplexers Mux1/2 and to dedicated analog switches. When the IC is in mission mode, each **D**-type pin is connected to the IC core via its switch closed and disconnected from ABM1/2 according to the proper neutral Mux1/2 address. For the in-circuit PCB level test purposes the **D**-type pins are isolated from the IC core by their switches opened, so become to be the "1149.4-probeable" pins that are usable for the in-circuit PCB level test purposes as they are connected to ABM1/2 (according to the proper multiplexer **D**-type pin address) for 1149.4 protocol implementation.

The **E-type** mixed-signal non-functional external I/O pins are not 1149.4-compliant, so have no functional usage when the IC is in mission mode. These in-circuit prober/injector pins are connected to Mux1/2, so become to be the "1149.4-probeable" pins and are usable for the in-circuit PCB level test purposes, as they are connected to ABM1/2 (according to the proper multiplexer **E**-type pin address) for 1149.4 protocol implementation.

The **F-type** mixed-signal non-functional internal I/O pins are not 1149.4-compliant too and have no functional usage when the IC is in mission mode. These in-core prober/injector pins are connected to Mux1/2 as well, so become to be the "1149.4-probeable" pins and are usable for the in-core test purposes of the IC, as they are connected to ABM1/2 (according to the proper multiplexer **F**-type pin address) for 1149.4 protocol implementation.

It should be emphasized that all cases of test usage of described pins do not effect neither the IC core nor the PCB mission mode while the above connections are made.

The BSR-2 of the Coder includes 1149.1- or 1149.4-compliant digital cells $\mathbf{D_A}$, connected via a buffer register to address inputs of analog multiplexers Mux1/2 and control inputs of analog switches of the **D**-type I/Os.

All I/O pins of types **B … F** are connected to multiplexers Mux1/2 inputs, separately to either or in parallel to both. There are five modes which make use of these I/O pins:

1) regular functional use of **B, C, D** types when the functional IC is in mission (normal functional) mode of operation;
2) use of **C, D, E** types for analog PCB node level test purposes and use of **B, D, E** types for digital PCB nodes level test purposes, such as in-circuit contactless signal voltage level or waveform delivery, digital and analog, in real time both for probing and for any signal insertion into the in-circuit PCB nodes;
3) use of **B, C, D, E** types for the PCB in-circuit contactless analog measurements;
4) use of **F** type for the IC in-core test purposes, such as the in-core contactless signal voltage level or waveform delivery, digital and analog, in real time both for probing and for any signal insertion into the IC functional core;
5) use of **F** type for the IC in-core contactless analog measurements.

When the IC with the described core DFT infrastructure is powered up, the buffer register connected to BSR-2 supplies hardwired address codes of **C** type pins to the address inputs of multiplexers Mux1/2, as well as hardwired close control signals to analog switches of **D** type pins. Both TAP-1 and TAP-2 are in a reset state in a regular 1149.1 or 1149.4-style, so the IC is ready to function in its mission mode.

On the first step of the IC usage for the in-circuit PCB level test purposes, the PRELOAD instruction of 1149.1 or 1149.4 is to be shifted into the IR of TAP-2 Coder circuitry, followed by the required address for analog multiplexers as well as the open control signals code for corresponding analog switches. This defines the required I/O pins of types **B … F** to be the "1149.4-probeable". These codes are captured and clamped in the BSR-2 after the CLAMP instruction is shifted into the IR of the TAP-2 circuitry, and then applied through buffer register to Mux1/2 address inputs and to corresponding switches control inputs.

On the next step the PROBE instruction is shifted into the IR of TAP-1 Prober circuitry, thus enabling TBIC and ABM1/2 switches as the 1149.4 protocol requires (Fig. 2) for the following test paths creation (according to Mux1/2 address inputs loaded):

AT1 <-> AB1 <-> ABM1 <-> Mux1 <-> selected **B … F** type pin
AT2 <-> AB2 <-> ABM2 <-> Mux2 <-> selected **B … F** type pin

Each such path is intended for probing or inserting signal levels or waveforms in real time both for the in-circuit PCB level test purposes and for the IC in-core test purposes, as well as for the in-circuit and in-core analog measurement purposes (see part 6). The functional IC continues to be in mission mode of operation when these paths are created.

The proposed embedded DFT infrastructure can facilitate the in-core voltages monitoring, e.g. in low-speed voltage converters (ADC, DAC), back-bias generators, reference voltages, as well as performing DC parametric tests, verifying that transistors are intact, measuring leakage current at inputs or tri-state outputs, etc. [10]. A lower cost probe card and tester can be used with minimal number of probes for testing hundreds of multiplexed IC pins and pins of a core internal logic and memory, thus reducing the cost of I/O testing.

The important feature of the proposed DFT infrastructure is its reusability, i.e. the infrastructure can be implemented as reusable design block in any IC design development.

The boundary-scan circuitry of a device with the proposed on-chip DFT infrastructure may be described in form of two serially connected separate devices with their BSDL files, each of them describes TAP-1 and TAP-2 circuitries.

5. Hardware verification

Experiments have been done on a prototyping hardware setup using two general purpose 1149.4 devices SCANSTA400 [6] in order to verify the feasibility of the Bridge-For-Testability structure (Fig. 5). The boundary-scan sequence is developed to control multiplexers Mux1/2 for switching two external analog buses AT1/2 to each one of eight external test points, TP0 through TP7, which are connected to a PCB in-circuit nodes-under-test. The SCANSTA400 ABM-TBIC switching is implemented by 1149.4 protocol via two selected device pins: pin A0 conveys AT1 bus to all TPs via multiplexer Mux1 and pin A1 conveys AT2 bus to all TPs via multiplexer Mux2. The functional cores of neither Prober nor Coder devices were used.

The following codes are the Prober device BSR conveying contents (LSB is closest to TDO):

100000400000h for AT1 <-> AB1 <-> A0 <-> Mux1 convey (switch SB1 of ABM1 enabled)
000200800000h for AT2 <-> AB2 <-> A1 <-> Mux2 convey (switch SB2 of ABM2 enabled)
100200C00000h for both AT1 <-> AB1 <-> A0 <-> Mux1 and
AT2 <-> AB2 <-> A1 <-> Mux2 convey (both switches SB1 and SB2 are enabled)

Address coding of both multiplexers was performed by shifting into the Coder device BSR and clamping (by 1149.1 or 1149.4 protocol) in the Coder BSR cells the appropriate conveying codes (LSB is closest to TDO):

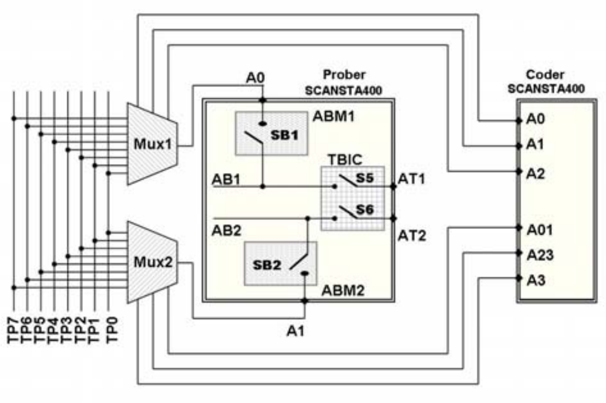

Fig. 5

Coder pins AA02 AA13 A23 A01	Mux Code	TP enabled
440440000404h	000	TP0
C404C0000404h	001	TP1
440C40000C04h	010	TP2
C40CC0000C04h	011	TP3
4C044000040Ch	100	TP4
CC04C000040Ch	101	TP5
4C0C40000C0Ch	110	TP6
CC0CC0000C0Ch	111	TP7

6. In-circuit testing approach vs. analog measurements

Number of papers [11,12] describe methods to determine values of discrete components (resistors, capacitors, etc.) and complex impedances calculated from measurement results obtained for different in-circuit connections, particularly in a case when a passive component or parallel RC circuit is connected between two pins of an 1149.4 device.

We will discuss the usage of the Bridge-For-Testability method described above as a basis for a simple and inexpensive approach to in-circuit passive discrete components testing in any schematic configuration. Let's say, nets V1 and V2 of an in-circuit impedance Z (it may be a single discrete component or any sub-circuit) are connected to a PCB external buses AT1/2 via the BFT circuitry as shown in Fig. 6, and the PCB is in mission mode with a real currents through nets V1 and V2. The real voltages $V1_{meas}$ and $V2_{meas}$ can be measured by any equipment manually or compared automatically with the expected voltages that have to be known prior to comparison. We can further download the digital comparator outputs via the 1149.1- or 1149.4-compliant BSR connected in the BFT chain.

If the BFT circuitry pins (input of Mux1/2) are connected to desirable for test in-circuit PCB nets, the digital signatures of expected voltages are saved in a database, and an ADC is connected to pins AT1/2, the comparison with data of the database makes the in-circuit passive components testing process fully automated.

There is no need in this approach to supply a known current into AT1 pin and measure voltage on AT2 pin, as it described in [10,11,12]. Moreover, no need to take into account the expected range of component values; to use accurate and expensive measurement instrumentation; and to develop automated test pattern generation tools for analog measurement implementation [11]. There is no need for a "guarding" setup as in the traditional ICT case, and the board-under-test may stay in the mission mode.

7. Discussion and conclusions

Analog signal contactless monitoring with use of the boundary-scan bus is valuable during all life cycle phases of a PCB: the board schematics development and debug, production, environmental, and field test, including analog measurement, embedded fault prediction and detection for high-availability systems. Combining 1149.1 and 1149.4 channels gives BFT device the ability to reach places on a PCB where boundary-scan could not reach on its own, not only extending boundary-scan structural test coverage significantly, but also adding functional test on the same test platform.

One of the reasons for the slow acceptance of 1149.4 is the comparison with the 1149.1 popularity, because the 1149.1 tools are fully computer based and require little or no additional hardware. The proposed BFT device alleviates well-known obstructions of 1149.4 wide use: the device requires simple external hardware (if any) and utilizes the on-the-shelf 1149.1 software tools. The BFT device would be relatively simple to integrate into an existing 1149.1 tool suites.

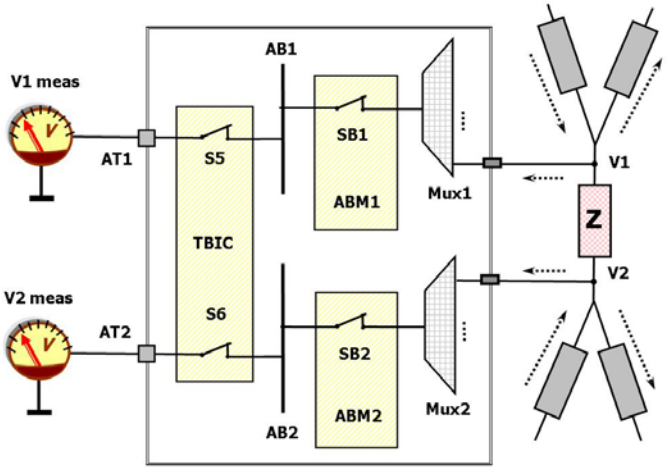

Fig. 6

The BFT IC is not fully 1149.4-compliant but it dismisses some of difficulties on the way of 1149.4 standard. As a standalone device, the BFT provides all capabilities of the 1149.4 during the PCB mission mode: analog and digital signal real-time monitoring and signal insertion, as well as in-circuit component testing with using only two ABMs and two analog multiplexers instead of dedicated ABM for each analog pin. Fault insertion in mixed-signal realm may be simply implemented for a large number of in-circuit injection points and be useful in inadequacy problem debug of conventional hardware and software tools [13].

Another 1149.4 problem is that most analog ICs tend to come in small pin count packages, and seven additional pins of 1149.4 become too high of a percentage [3]. This obstacle may be eliminated by external contactless probing of mixed-signal IC pins or PCB in-circuit nodes with the described BFT device.

The need to test on-board power nodes has been discussed in [10] and it was highlighted that the connectivity defects on such nodes are relatively common and are very difficult to detect. The proposed method and specific BFT IC facilitate remote probing on physically non-accessible or difficult-to-access analog and digital nodes in a PCB. Further research has to be made to find flexible DFT rules for selecting optimal in-circuit probing points and maximizing the PCB fault coverage.

The 1149.4 analog bus is specified to have a frequency range of about 100 kHz or a little more which may be insufficient to test many digital and analog signals. Nevertheless, most impedance measurements are done at frequencies below 10 kHz to minimize noise effects. The technique described here will use sub-megahertz frequencies on the analog bus too. When monitoring signals in continuous time via the analog multiplexers, the maximum bandwidth is limited by the capacitance of the signal conveying nodes. Such analog buffer is much closer to the circuit probing node than a buffer of an external tester, and as such, it can reduce the parasitic capacitance to less than 15 pF instead of the 50-100 pF as typical for many testers [1].

Not so wide usage of 1149.4 in IC production test is explained by several reasons, particularly by silicon real estate costs for implementation of many ABMs [14]. In addition, the reduced pin count test (RPCT) is becoming popular as a way of keeping down the cost of test for ICs that are “fully loaded” with internal scan, BIST or 1149.1. The proposed embedded mixed-signal core DFT infrastructure with reduced number of ABMs may be used to quickly generate tests for analog in-core clusters, as well as for RPCT implementation during low-frequency in-core I/Os wafer probe by reducing both cost and contact problems [15], and enable AC/DC parametric testing with only a few high-speed, high resolution pins needed (clocks, etc). The proposed method may be quite suitable for logic core and embedded memories testing in design and early production stages when any design deviations are acceptable. In the final IC packaged configuration the number of in-core I/Os connected to BFT multiplexers may be reduced.

The modern IC design cost increase exponentially, so the Design-For-Testable-Reuse (DFTR) is a vital economic requirement to allow pre-existing test functions to be efficiently integrated into new devices. The described core DFT may be utilizing in IEEE 1500-compliant SOC [16] as part of the hierarchical reusable boundary-scan test wrapper system.

8. Acknowledgement

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