



BTU 2003
Board Test Workshop 2003

Remote Diagnostics and Upgrades

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About this Presentation

- Motivation for Remote Diagnostics
 - Reduce Field Maintenance costs
 - Product needed to support 100 JTAG chains
 - Support non-compliant vendors
- Scope
 - will not discuss remote access SW schemes
 - will address detailed System Level JTAG
- Terminology
 - Reconfiguration vs Reprogramming

Agenda

- Remote Diagnostics Example
- Benefits
- JTAG MUX IP
- Remote Diagnostics Board Overview
- Altera EPC ISP configuration proms
- Embedded FPGA BIST Controller
- JTAG Signal Integrity
- Summary

Remote Diagnostics/ Upgrade Example

Remote JTAG Enabled Product

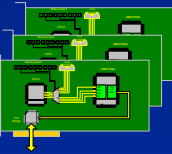
Programming/
Test Files



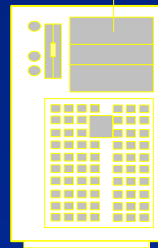
Software
JTAG
Controller



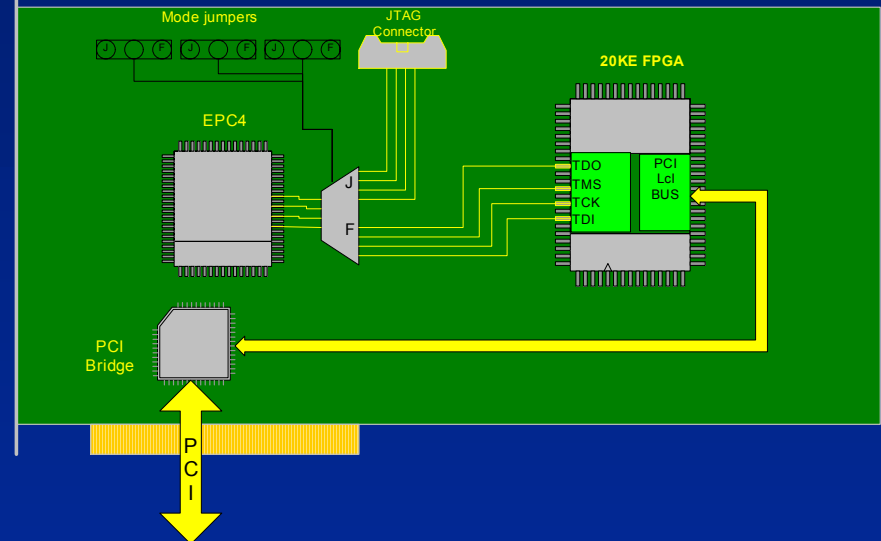
System Level
JTAG Access



Remote
Access



Product



- JTAG access to all chains in the system with a single point of entry (Ideal)
- Embedded JTAG controller with Test and/or programming files
- Remote Access can control product or download updated files

Benefits - Remote Diagnostics/Upgrades

- \$\$\$
 - Test Development Reuse
 - Reduction in Field Service Labor
 - Simple enough for end user test/updates
 - Remote test/updates
- Time
 - Time to market improved
 - less JTAG debug needed
 - latest FW can be upgraded in the field
 - Better Uptime
 - Remote diagnostics isolate fault so replacement part is in hand.
 - Timely upgrades

Benefits- Reduction in Field Service labor

Traditional Field Service (FS)

Update Labor time = 20,000 hrs or 500 wk

(5000 products) (4 hrs/ products)

Update cost = \$1.5 Million (per upgrade)

(20,000 hrs) (\$75/hr)

Remote Upgrade

Update Labor Time time = 1hr

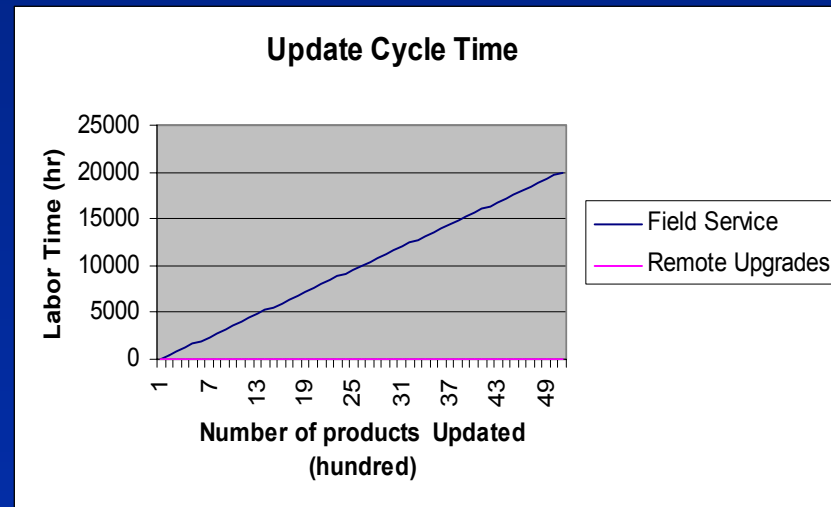
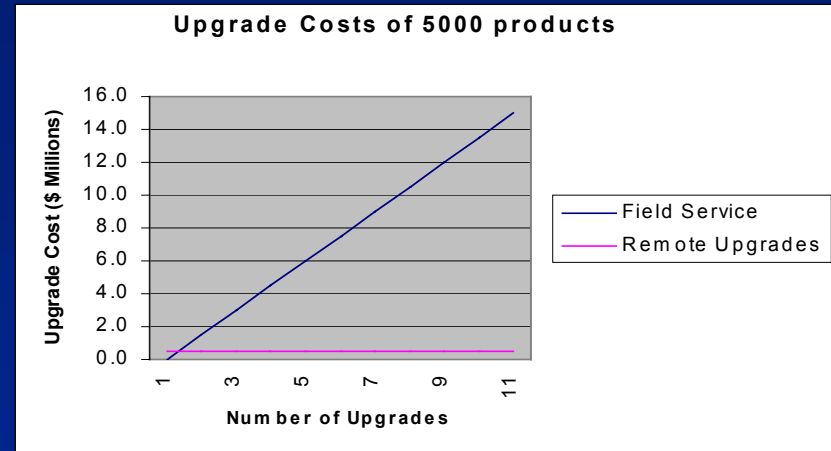
Development cost = \$400k

(2 Engineer yrs.) (2000hr /yr..) (\$100/hr)

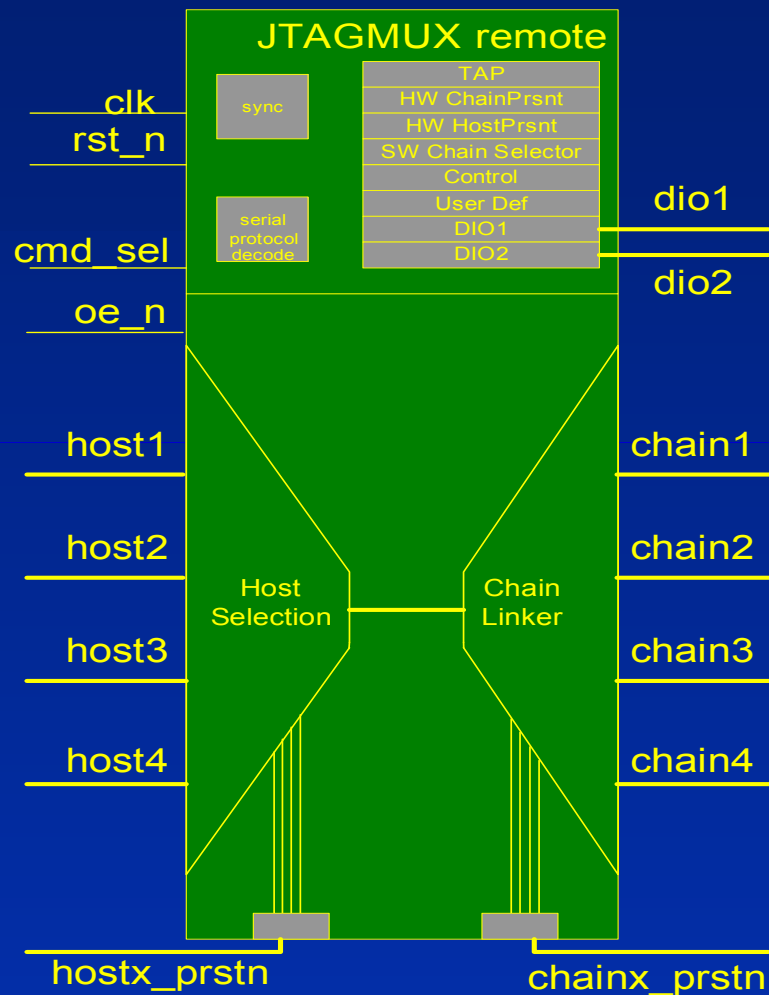
Hardware cost = \$100k

(5000 prod) (\$20 / prod)

Total Upgrade cost = \$500k (one time cost)



JTAG MUX IP Overview



JTAGMUX remote -

uses a serial protocol to write or read JTAG registers via software control

The JTAG registers allow control of the chain and hosts regardless of Host and chain present inputs

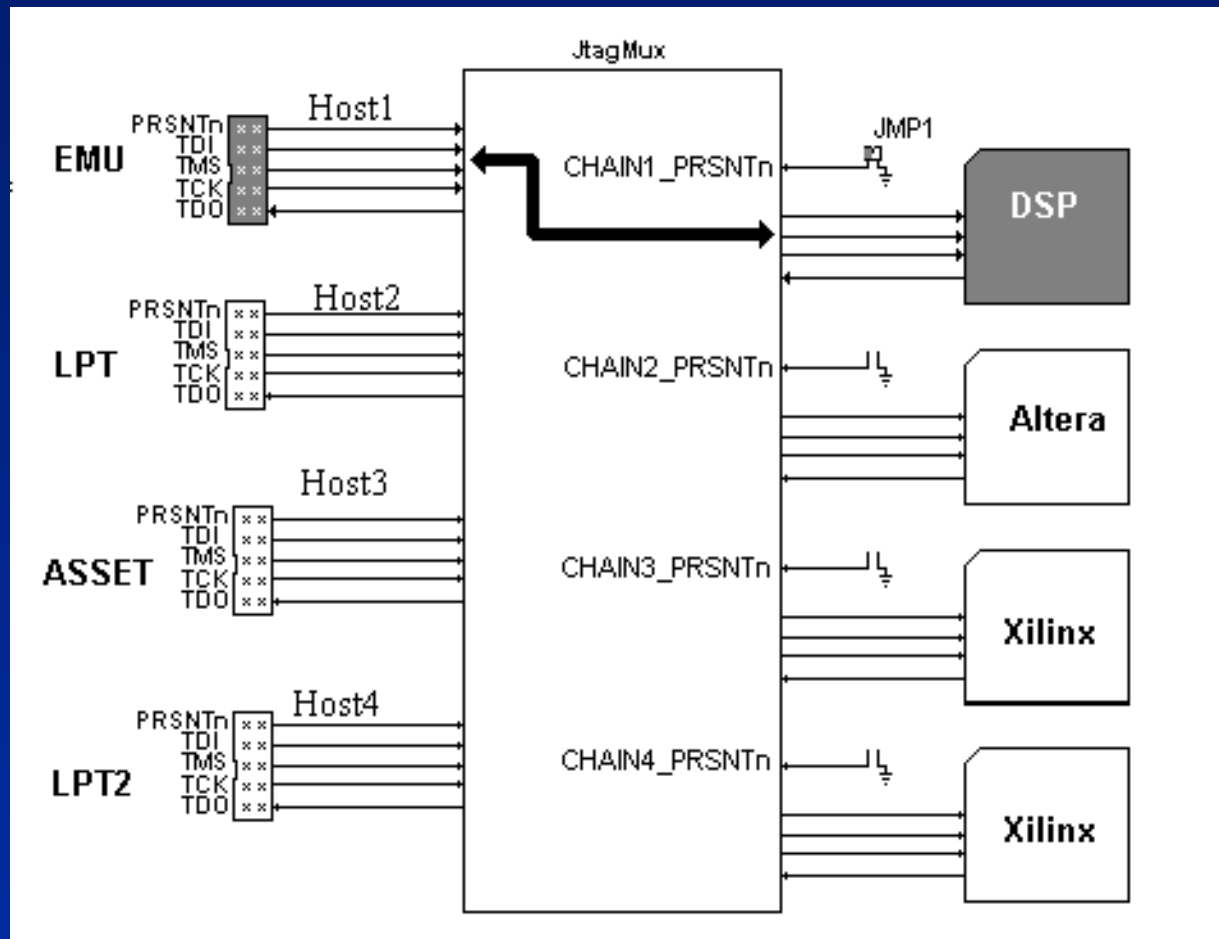
JTAGMUX local-

The Host Selection and Chain linking is dependant on the Host and Chain present inputs

Host priority host1 highest & host4 lowest (incase of multiple hosts)

Chain order is guaranteed chain1 first & chain 4 last

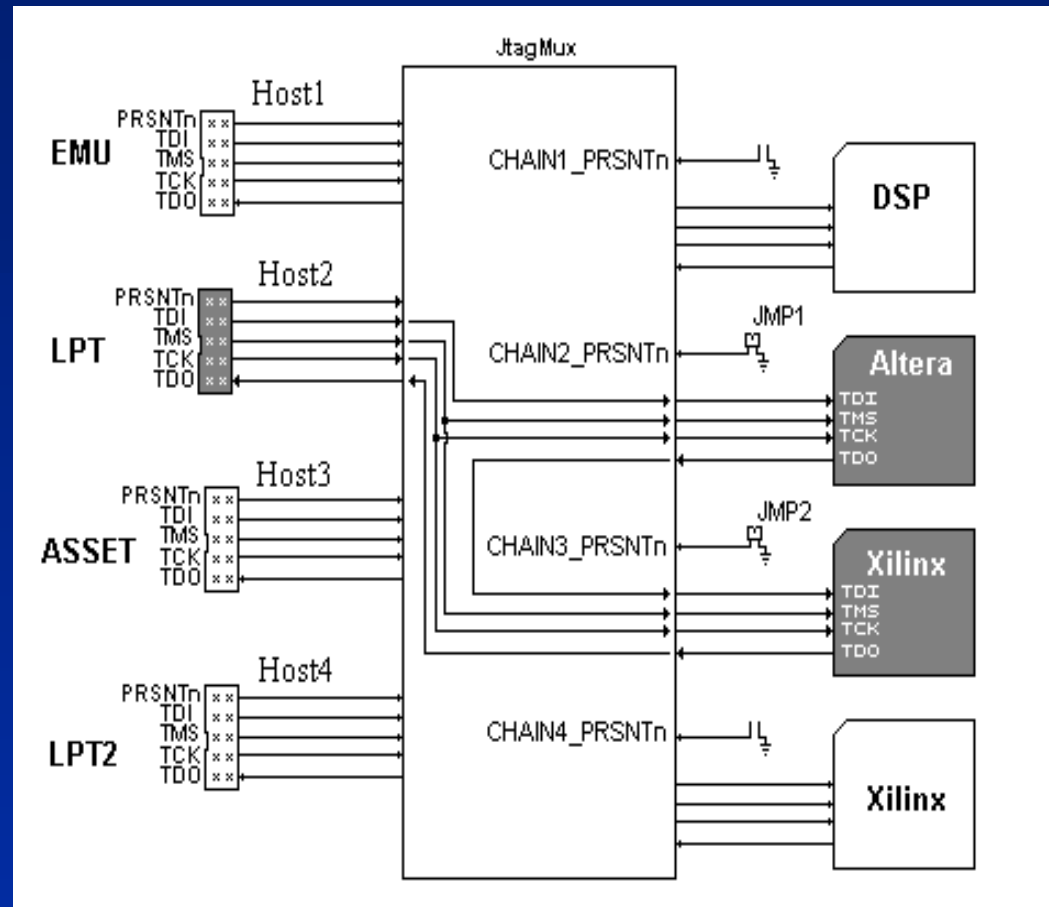
JTAG MUX local - isolating a chain



Chain isolation is important, many silicon vendors have non-compliant JTAG hardware or software

Emulator Host drives the DSP, chain1 is selected because chain1 Present pin is connected to ground through JMP1.

JTAG MUX local - daisy chain



Altera and Xilinx devices are daisy-chained, chain1&2 Present pins are connected to ground through JMP1 & JMP2.

Automatic Chain Selection/ Host Adapter Harness

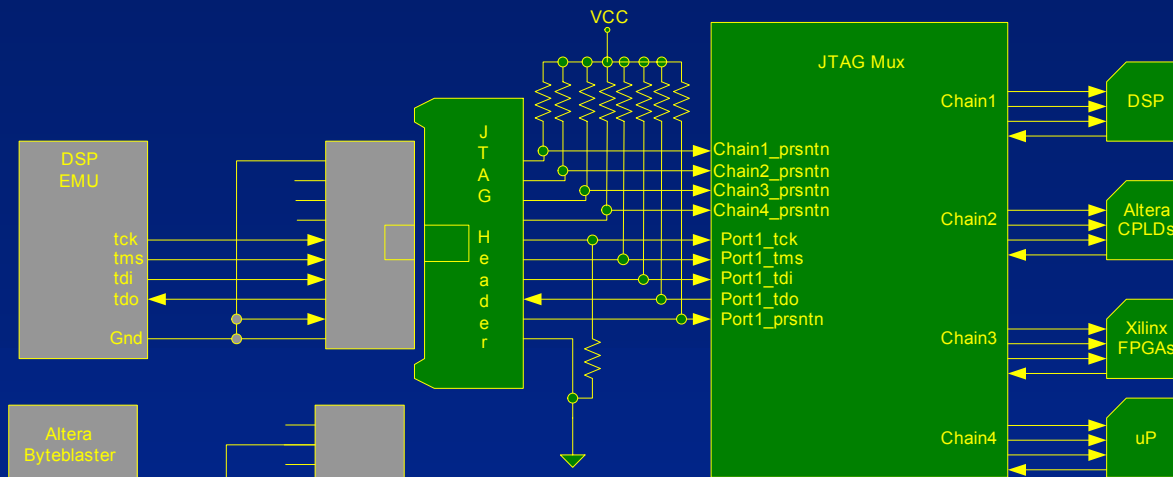


Illustration of Reducing the number of JTAG connectors on a Board.

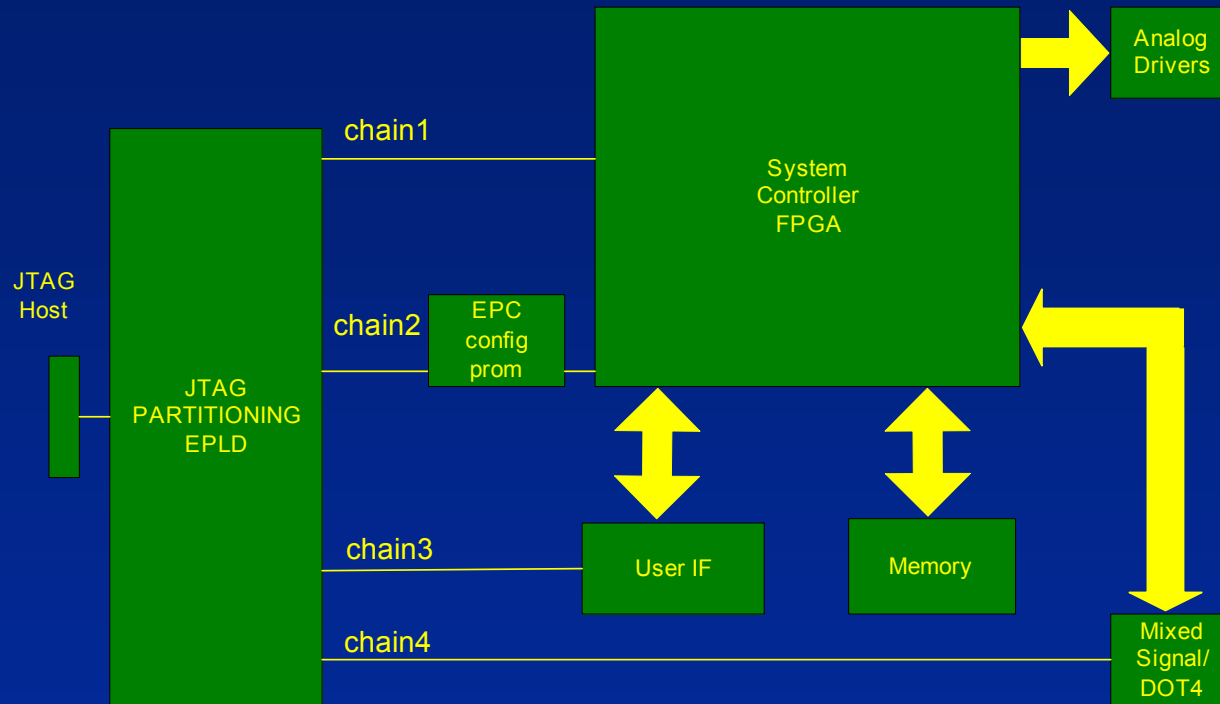
Create one JTAG connector on the board.

Create a harness that adapts each JTAG host to the JTAG connector.

The appropriate chain is automatically selected because the harness routes ground to the corresponding chain present line, no jumpers needed.

Note the Asset JTAG tester has optimal control since it has digital io pins

Remote Diagnostics Board (RDB) Block Diagram



Chain1 is connected to IO pins on the FPGA and depending on the configuration loaded may or may not have soft TAP functionality.

Chain 2 has two devices, the Altera EPC4 and FPGA.

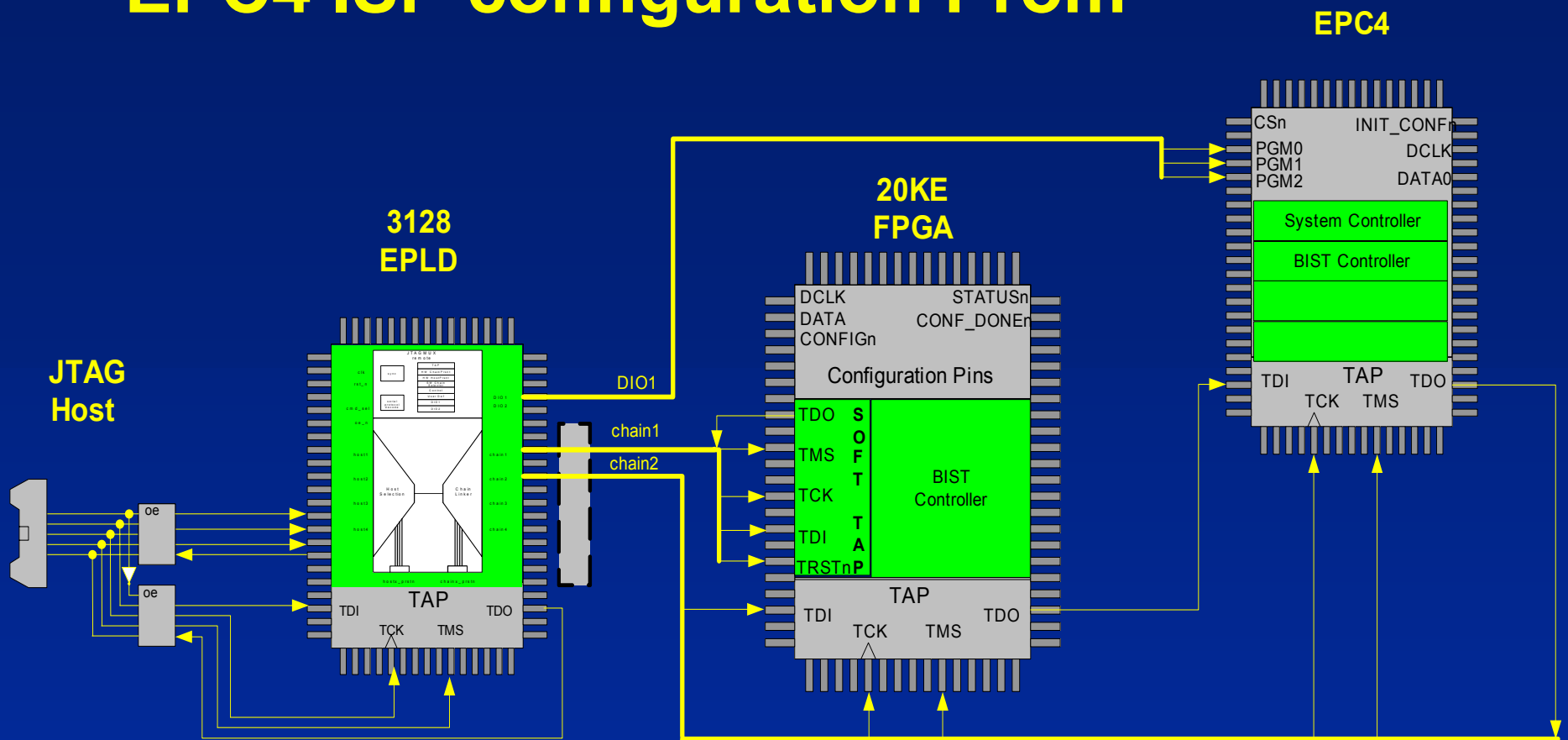
Chain 3 consists of three 74abt18245 buffers.

Chain 4 is a National Semiconductor STA400 Dot 4 chip.

Embedded FPGA BIST Controller

- Use the Centralized FPGA to Test the board at speed
- BIST routines were developed for FPGA peripherals
 - (SRAM, Relays, Fans, Stepper Motor, ADC)
- MemBIST VHDL generated by Mentor SW
- Mentor BSD Architect developed a soft TAP VHDL JTAG interface
- New instructions were added to soft tap to launch the Test Benches.

EPC4 ISP configuration Prom

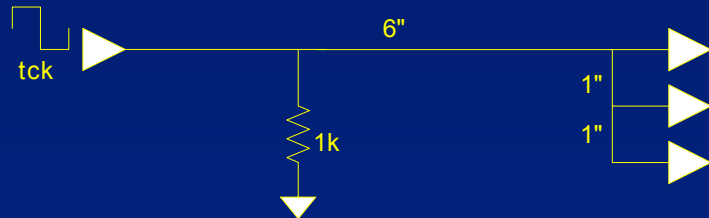


System level JTAG - All chains are accounted for. The JTAG host can access the JTAG MUX host4 input to gain access to chains 1- 4 (only 1&2 shown).

The JTAG host can also access the EPLD TAP for reprogramming .

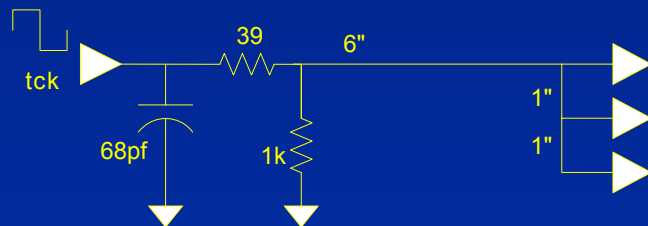
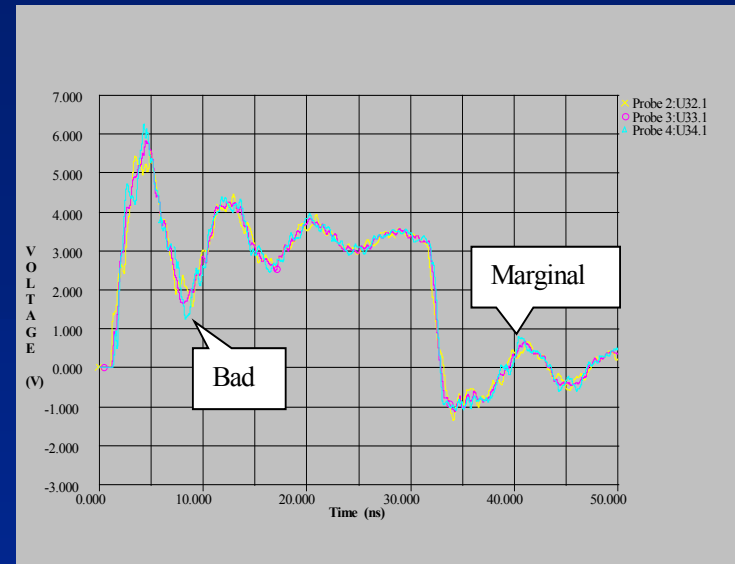
The EPC4 will configure the FPGA with the page of memory corresponding to PGM pins driven by the JTAG MUX.

TCK Signal Integrity

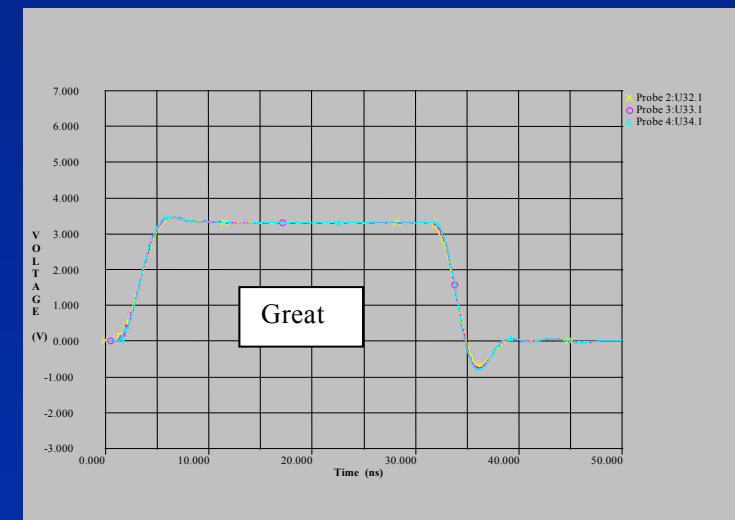


NO COMPENSATION

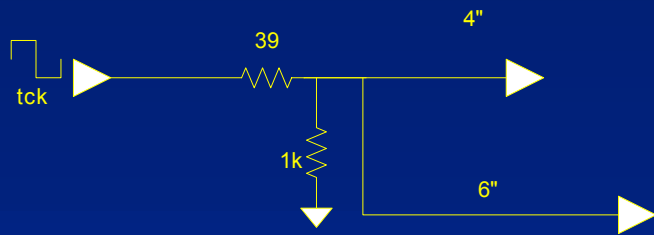
The waveform shows fluctuations on TCK upper rail into intermediate area for about 3ns (BAD). Fluctuations at the lower rail are marginal since they exceed .8v for less than 1ns.



SERIES COMPENSATION & CAP The capacitor at the output of the driver slows the rise time down to from 1ns to 3.5 ns.

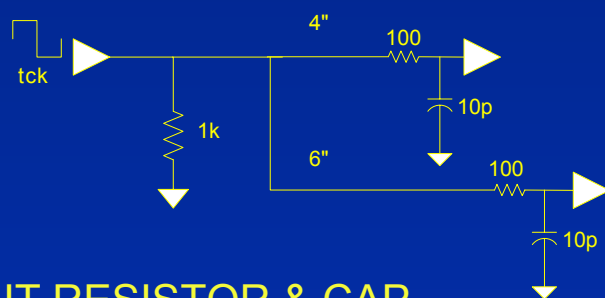
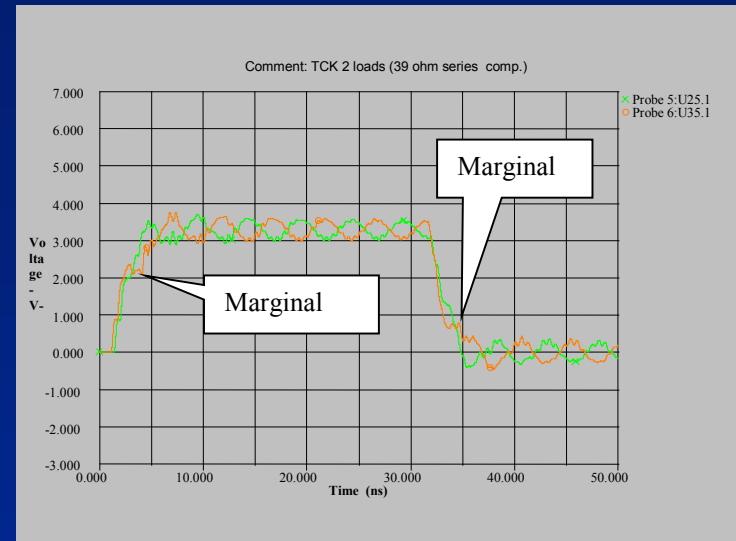


TCK Signal Integrity



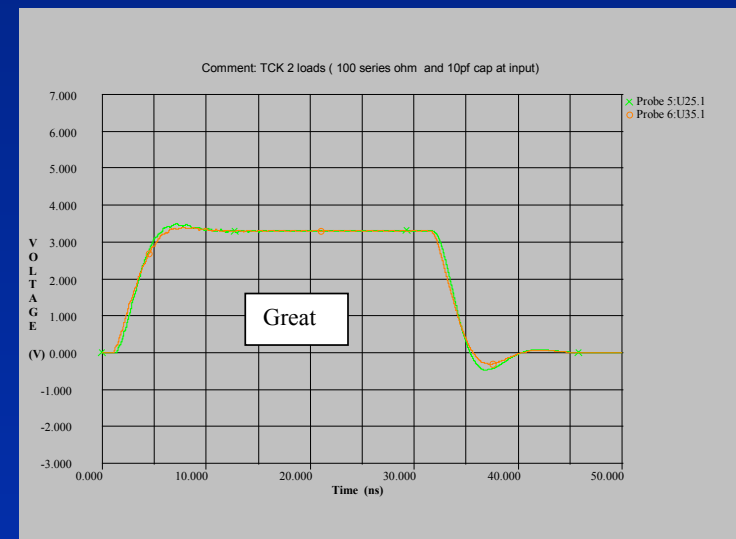
SERIES COMPENSATION

Adding compensation made the both edges look worse, however it did help the ringing slightly.



INPUT RESISTOR & CAP

The new C value is 10pf + C_{in} which slows the edges down even further.



Summary

- Treat TCK like any other clock signal for SI
- A System level JTAG strategy enables Remote diagnostics and upgrades
 - JTAG MUX
 - Embedded BIST in FPGAs allows HW engineers to test the hardware
- Concerns with Remote operations
 - Security / Remote Access method
 - Safety
- Huge Benefits \$\$

Acronyms

- BIST Built In Self Test
- EPLD Electrically Programmable Logic Device
- EMU Emulator
- FPGA Field Programmable Gate array
- FS Field Service
- FW Firmware
- HW Hardware
- IP Intellectual Property
- ISP In-System Programmable
- JAM Altera developed Standard Test and Programming Language
- JTAG Joint Test Action Group, IEEE1149.1
- LPT PC Parallel Port
- PCB Printed Circuit Board
- SI Signal Integrity
- STPL Standard Test and Programming Language (JEDEC JESD71)
- SVF Serial Vector Format
- SW Software