

# CPLD REPROGRAMMING – A PRACTICAL APPLICATION OF AN 1149.1 BACKPLANE BUS

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## Abstract

Increasing the permeation of boundary scan from boards to systems improves test and programming access, enabling more options that can be exercised throughout the life of a product. By proper partitioning of the system, boundary scan lends itself to re-use of the factory test and programming vectors. This is especially useful for cPLD reprogramming in the field support application. Ensuring that access to the boundary scan “port” is available while requiring that the design be compatible with in-system programming can result in new applications of the standard technology that add value to a product without significantly impacting cost.

## Access

Achieving boundary scan field reprogramming of an ISP device requires access to the device’s 1149.1 TAP. This access, referred to in this paper as system-level access, enables a controlling device to provide the reprogramming vectors to the target part. This is usually done via a simple hardware interface such as a header or similar connector with the controlling entity being the hardware and software of the boundary

scan developer’s ATPG tool. For self-contained and automated tests, however, this system-level access can be integrated into the functionality of the product, requiring no external connections to third-party tools.

## Components

Integration of the capability for system-level reprogramming of a target cPLD has been designed into a Motorola cellular infrastructure base station Site Master (host) card. The hardware of the card incorporates a scan chain partitioning device (Gateway) mandated by production for easing test concerns, and a boundary scan Controller device. The Controller interfaces with the microprocessor of the host card, thus taking the place of the ATPG tool’s vector pump.

Coupled with test software drivers integrated into the functional software of the host card, this system-level solution supplied by Firecron Limited provides boundary scan functionality approaching that of production boundary scan ATPG tools. With this, a fully automated application has emerged that proves useful for field upgrade of cPLD cores. See Figure 1.

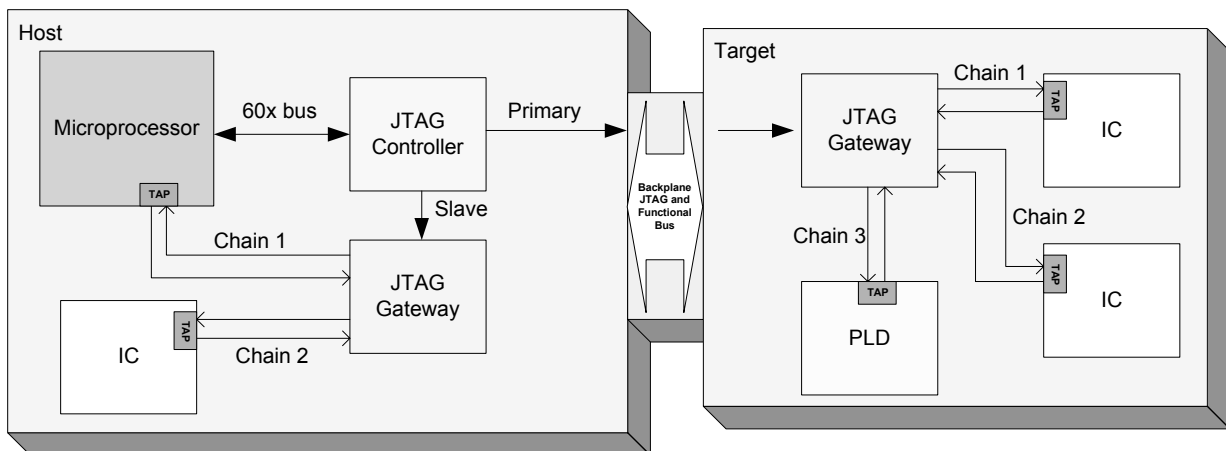
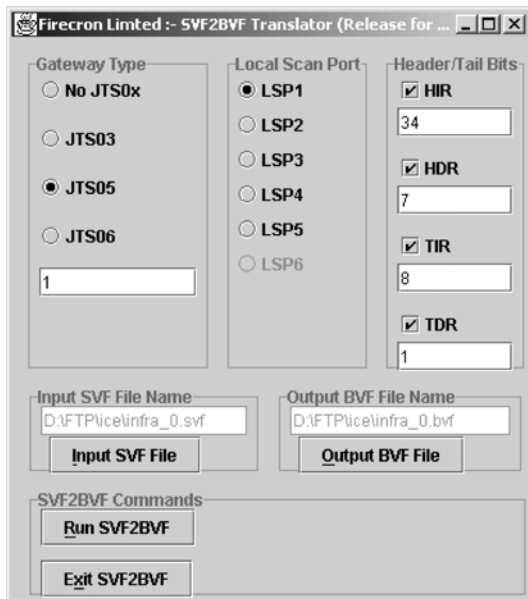


Figure 1

A common programming method for cPLDs is the Serial Vector Format (SVF) file. This file contains the core image to be programmed as well as the 1149.1 overhead for setting up the target device. It is also possible to indicate in this SVF file the other parts on the scan chain the target device is on, although this is not necessary for the system-level tools that are discussed here.

The Firecron Controller uses a proprietary Binary Vector Format (BVF) file, requiring initial SVF file conversion. (This is where other devices on the scan chain can be declared if not already done so in the SVF file. See Figure 2.)



**Figure 2**

Once conversion is achieved, the BVF file is stored on the host card as a file in the functional file system or other software accessible location. Typical storage locations are the flash used for application software of the host card. Using a software command either under the host card’s diagnostic/maintenance software or manually entered via a terminal interface, the Firecron Controller driver is invoked and passed the BVF file. The BVF file contains the core image as well as the necessary protocol to set up the Gateway device to access the particular scan chain that the target cPLD is on. Processing of the BVF file completes with user specified options, including the TCK speed, and Gateway addressing. Successful completion will result in a re-programmed cPLD.

Output generated by execution will indicate failures depending on the verbosity specified in the parameters, although SVF reprogramming of cPLDs is typically limited to Pass/Fail criteria. If a series of test or programming functions must be completed, a plain-text script can be generated to pass all necessary parameters to the Firecron application, further automating the process.

### Concerns

A key component to achieving a system-level boundary scan approach involves verifying the integrity of the scan chain to the target device. Due to poor implementations of 1149.1 in the several devices that exist on scan chains, it is possible that the entire target card’s functionality must be interrupted to enable a contiguous chain. As long as the target card is not the same card that is executing the vectors to attempt the programming, it is sufficient to keep this concern in mind.

An interesting side concern here is ensuring that the requirements from production test don’t limit the ability of the system-level reprogramming to function as transparently as possible. This can surface when reusing scan chain multiplexers or ensuring safe states by assertion of a “boundary scan active” signal. If the host card running the system-level boundary scan incorporates these features in support of production test, the host card must have a method of distinguishing between a production boundary scan state and a field boundary scan state.

Aside from the functional concerns of how to initiate reprogramming, additional difficulties in achieving this involve the intrusive nature of 1149.1 access, particularly as it relates to cPLDs. Typically, cPLDs contain important “glue logic”, and oftentimes reset control logic. During reprogramming, target cPLDs will “safe” its I/O, possibly causing the target card to enter an unknown state as well as resetting whatever functional logic was just applied. For this reason, it is desirable to have the capability to reset the target card at whatever level is required to bring the board up in a usable state. This can be automatic upon exiting the boundary scan state based on the reset structure of the target card, or initiated by a Master card. In the case of this example, both mechanisms are present, allowing for a two-level recovery feature.

## **Use**

If fully automated re-programming is not possible or desirable, the system-level boundary scan approach can still be extremely useful for human-controlled field servicing. Under this scenario, a field support agent visiting a site would not require special interface hardware or software. With the functionality built into the card, a simple terminal interface and file server can be used to upload the update core image and initiate the vector processing.

Although not explicitly designed for it, system-level applications of IEEE 1149.1 are proving useful for properly designed systems to take advantage of the standardized interface. With the development of chipset solutions and the associated drivers and software to maximize the possibilities of boundary scan reuse, designers can make available to field diagnostic/maintenance entities the boundary scan capabilities that has traditionally been lost when the product exits the production floor.

## **Reference**

Harrison, Noeninckx, Horwood, Collins:  
“Hierarchical Boundary-Scan, A Scan Chip-Set Solution”, IEEE ITC 2001 (Paper 17.2)